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APPENDIX C

(CLEAN VERSION OF ALL PENDING CLAIMS)

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CLAIMS

What is claimed is:

1. A method for disposing a material on a semiconductor device structure, comprising:

providing a semiconductor device structure including a surface and at least one recess formed in said surface;

disposing the material on said surface so as to substantially fill said at least one recess, the material covering said surface having a thickness less than a depth of said at least one recess without subsequently removing the material from over said surface.

2. The method of claim 1, wherein said disposing comprises disposing the material so as to substantially fill the at least one recess without substantially covering said surface.

3. The method of claim 1, wherein said disposing comprises:

applying the material to said surface of said semiconductor device structure;

spinning said semiconductor device structure;

decreasing a rate of said spinning while permitting the material to at least partially cure; and

gradually increasing said rate of said spinning.

4. The method of claim 3, further comprising exposing the material to a soft baking temperature following said gradually increasing.

5. The method of claim 3, wherein said spinning is effected at a rate of about 1,000 rpm.

6. The method of claim 3, wherein said decreasing said rate comprises decreasing said rate of said spinning to about 100 rpm.

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7. The method of claim 3, wherein said gradually increasing said rate comprises gradually increasing said rate of said spinning to at least about 1,000 rpm.

8. The method of claim 1, wherein, upon exposing the material disposed over an entirety of said semiconductor device structure to an etchant, the material covering said surface is substantially removed therefrom, while the material located in said at least one recess substantially fills said at least one recess.

9. The method of claim 1, wherein said providing said semiconductor device structure comprises providing a stacked capacitor structure with said at least one recess comprising at least one container formed in an insulator layer of said stacked capacitor structure, said surface and said at least one container being lined with a conductive material.

10. The method of claim 9, wherein said providing said semiconductor device structure comprises providing said stacked capacitor structure with said surface and said at least one container being lined with doped hemispherical grain polysilicon.

11. The method of claim 9, wherein said disposing the material comprises disposing a mask material over said semiconductor device structure.

12. The method of claim 1, wherein said providing said semiconductor device structure comprises providing a shallow trench isolation structure with said at least one recess comprising at least one trench formed in a surface of said shallow trench isolation structure.

13. (Amended) The method of claim 12, wherein said disposing the material comprises disposing a mask material over said shallow trench isolation structure.

14. (Amended) The method of claim 12, wherein said providing said shallow trench isolation structure comprises providing said shallow trench isolation structure with an insulator layer substantially filling said at least one trench and covering said surface.

15. The method of claim 14, wherein said disposing the material comprises disposing a stress buffer over said insulator layer, said stress buffer having a substantially planar surface without removing material thereof following said disposing.

16. The method of claim 1, wherein said providing comprises providing a semiconductor device structure having a surface with at least one dual damascene trench recessed therein and a layer of conductive material with a nonplanar surface disposed in said at least one dual damascene trench and at least partially covering said surface.

17. The method of claim 16, wherein said disposing the material comprises disposing a stress buffer over said layer of conductive material, said stress buffer having a substantially planar surface without removing material thereof following said disposing.

18. A method for masking a stacked capacitor structure, comprising:

providing a semiconductor device structure with a stacked capacitor structure including:

an insulator layer;

at least one container formed in said insulator layer; and

a layer of conductive material covering a surface of said insulator layer and lining said at least one container;

applying a layer of masked material to said semiconductor device structure; and

spreading said mask material across said semiconductor device structure so as to substantially fill said at least one container and cover said layer of conductive material over said surface with a thickness of about less than half a depth of said at least one container.

19. The method of claim 18, wherein said providing said semiconductor device structure comprises providing a semiconductor device structure with said layer of conductive material of said stacked capacitor structure comprising hemispherical grain polysilicon.

20. The method of claim 18, wherein said spreading comprises spinning said mask material across said semiconductor device structure.

21. The method of claim 20, wherein said spinning comprises:
rotating said semiconductor device structure at a first speed;
decreasing a rate of said rotating to a second speed; and
gradually increasing said rate of said rotating to a third speed.

22. The method of claim 21, wherein said decreasing said rate follows said rotating.

23. The method of claim 22, wherein said gradually increasing said rate follows said decreasing said rate.

24. (Amended) The method of claim 18, wherein said spreading comprises substantially filling said at least one container with said mask material while leaving said layer of conductive material covering said surface substantially uncovered by said mask material.

25. (Amended) The method of claim 18, further comprising removing said layer of conductive material covering said surface.

26. The method of claim 25, wherein said removing comprises etching said layer of conductive material.

27. The method of claim 26, wherein said etching comprises wet etching said layer of conductive material.

28. The method of claim 26, wherein said etching comprises dry etching said layer of conductive material.

29. The method of claim 25, wherein during said removing said at least one container remains substantially filled with said mask material.

30. The method of claim 25, further comprising removing said mask material from said at least one container.

31. (Amended) A method for forming a shallow trench isolation structure, comprising:

providing a semiconductor substrate with a surface and at least one shallow trench recessed in said surface;

applying mask material to said semiconductor substrate;

spreading said mask material across said semiconductor substrate so as to substantially fill said at least one shallow trench, said mask material covering said surface as a result of said spreading having a thickness of less than about half a depth of said at least one shallow trench; and

exposing at least said mask material to a dopant so as to conductively dope semiconductor material beneath said surface without substantially doping semiconductor material located beneath said at least one shallow trench.

32. The method of claim 31, wherein said spreading comprises spinning said mask material across said semiconductor substrate.

33. The method of claim 32, wherein said spinning comprises:

rotating said semiconductor substrate at a first speed;

decreasing a rate of said rotating to a second speed; and

gradually increasing said rate of said rotating to a third speed.

34. The method of claim 33, wherein said decreasing said rate follows said rotating.

35. The method of claim 34, wherein said gradually increasing said rate follows said decreasing said rate.

36. (Amended) The method of claim 31, wherein said spreading comprises substantially filling said at least one shallow trench with said mask material while leaving said surface substantially uncovered by said mask material.

37. (Amended) The method of claim 31, wherein said exposing includes implanting conductivity dopant into regions of said semiconductor substrate continuous with said surface without implanting conductivity dopant into regions of said semiconductor substrate continuous with a bottom of said at least one shallow trench.

38. The method of claim 31, further comprising removing said mask material from said semiconductor substrate.

39. (Amended) A method for fabricating a semiconductor device structure, comprising:

providing a semiconductor device structure with a surface, at least one recess formed in said surface, and a material layer at least partially covering said surface and substantially filling said at least one recess, said material layer having a nonplanar surface;

applying a stress buffer material to said material layer; and

spreading said stress buffer material over said material layer so as to impart said stress buffer material with a substantially planar surface without subsequently planarizing said stress buffer material.

40. The method of claim 39, wherein said providing comprises providing said semiconductor device structure with said nonplanar surface of said material layer including at least one peak located substantially over said surface and at least one valley located substantially over said at least one recess.

41. The method of claim 39, wherein said spreading comprises spinning said stress buffer material across said semiconductor device structure.

42. The method of claim 41, wherein said spinning comprises:
rotating said semiconductor device structure at a first speed;
decreasing a rate of said rotating to a second speed; and
gradually increasing said rate of said rotating to a third speed.

43. The method of claim 42, wherein said decreasing said rate follows said rotating.

44. The method of claim 43, wherein said gradually increasing said rate follows said decreasing said rate.

45. The method of claim 40, wherein said spreading comprises at least partially filling said at least one valley with said stress buffer material while leaving said at least one peak substantially uncovered by said stress buffer material.

46. The method of claim 45, further comprising planarizing at least said material layer.

47. The method of claim 46, wherein said planarizing comprises etching at least one region of said material layer exposed through said stress buffer material with selectivity over said stress buffer material.

48. (Amended) The method of claim 47, wherein said etching is effected until a surface of said at least one region is in substantially the same plane as said substantially planar surface of said stress buffer material.

49. (Amended) The method of claim 48, wherein said planarizing further comprises abrasively planarizing said stress buffer material and said at least one region to expose said surface adjacent said at least one recess, said surface and a surface of material in said at least one recess being located in substantially the same plane following said planarizing.

50. The method of claim 48, wherein said planarizing further comprises concurrently etching said material layer and said stress buffer material at substantially the same rate so as to expose said surface adjacent said at least one recess with said surface and a surface of material in said at least one recess being located in substantially the same plane following said planarizing.

51. The method of claim 47, wherein said etching is effected until said surface of said semiconductor device structure is exposed through said material layer.

52. The method of claim 51, wherein said etching is effected until a surface of material in said at least one recess is in substantially the same plane as said surface.

53. The method of claim 51, further comprising removing said stress buffer material from said semiconductor device structure.

54. The method of claim 40, wherein said spreading comprises forming a substantially planar surface over said semiconductor device structure.

55. The method of claim 54, further comprising planarizing at least said material layer.

56. (Amended) The method of claim 55, wherein said planarizing comprises substantially concurrently abrasively planarizing said stress buffer material and said material layer to expose said surface adjacent said at least one recess, said surface and a surface of material in said at least one recess being located in substantially the same plane following said planarizing.

57. The method of claim 55, wherein said planarizing comprises substantially concurrently etching said material layer and said stress buffer material at substantially the same rate so as to expose said surface adjacent said at least one recess with said surface and a surface of material in said at least one recess being located in substantially the same plane following said planarizing.

58. The method of claim 39, wherein said providing said semiconductor device structure comprises providing a shallow trench isolation structure with said at least one recess comprising at least one trench and said material layer comprising electrical insulator material.

59. (Amended) The method of claim 39, wherein said providing comprises providing a semiconductor device structure with at least one recess comprising a dual damascene trench and said material layer comprising conductive material.

60. A method for preparing a surface of a semiconductor device structure for planarization, comprising:

providing a semiconductor device structure including at least one recess formed in a surface thereof and a first material layer substantially filling said at least one recess and covering said surface, said first material layer having a nonplanar surface;

applying a second material to said first material layer; and

spreading said second material over said first material layer so as to form a second material layer having a substantially planar surface without requiring subsequent planarization of said second material.

61. The method of claim 60, wherein said applying said second material comprises applying a layer of stress buffer material to said first material layer.

62. The method of claim 60, wherein said spreading comprises:
spinning said semiconductor device structure at a first speed;
gradually decreasing a rate of said spinning to a second speed; and
gradually increasing a rate of said spinning to a third speed.

63. The method of claim 62, wherein spinning said semiconductor device structure at said second speed comprises permitting said second material within said at least one recess to at least partially set.

64. The method of claim 62, wherein spinning said semiconductor device structure at said third speed comprises forming said second material over said surface to a desired thickness.

65. The method of claim 60, wherein said providing comprises providing a shallow trench isolation structure with said at least one recess comprising at least one trench formed in a surface of said shallow trench isolation structure.

66. (Amended) The method of claim 65, wherein said providing further comprises providing said shallow trench isolation structure with said first material layer comprising an electrical insulator material.

67. The method of claim 60, wherein said providing comprises providing a semiconductor device structure with said at least one recess comprising at least one dual damascene trench formed therein.

68. The method of claim 67, wherein said providing further comprises providing a semiconductor device structure with said first material layer comprising conductive material.

69. The method of claim 61, wherein said spreading comprises at least partially filling at least one valley of said first material layer with said stress buffer material while leaving at least one peak of said first material layer substantially uncovered by said stress buffer material.

70. The method of claim 69, further comprising planarizing at least said first material layer.

71. The method of claim 70, wherein said planarizing comprises etching at least one region of said first material layer exposed through said stress buffer material with selectivity over said stress buffer material.

72. (Amended) The method of claim 71, wherein said etching is effected until a surface of said at least one region is in substantially the same plane as a surface of said stress buffer material.

73. (Amended) The method of claim 72, wherein said planarizing further comprises abrasively planarizing said stress buffer material and said at least one region to expose said surface of said semiconductor device structure adjacent said at least one recess, said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing.

74. (Amended) The method of claim 72, wherein said planarizing further comprises concurrently etching said first material layer and said stress buffer material at substantially the same rate so as to expose said surface of said semiconductor device structure adjacent said at least one recess with said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing.

75. The method of claim 71, wherein said etching is effected until said surface of said semiconductor device structure is exposed through said first material layer.

76. (Amended) The method of claim 75, wherein said etching is effected until a surface of said first material layer in said at least one recess is in substantially the same plane as said surface of said semiconductor device structure.

77. The method of claim 75, further comprising removing said stress buffer material from said semiconductor device structure.

78. The method of claim 61, wherein said spreading comprises forming a substantially planar surface over said semiconductor device structure.

79. The method of claim 78, further comprising planarizing at least said first material layer.

80. (Amended) The method of claim 79, wherein said planarizing comprises substantially concurrently abrasively planarizing said stress buffer material and said first material layer to expose said surface of said semiconductor device structure adjacent said at least one recess, said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing.

81. (Amended) The method of claim 79, wherein said planarizing comprises substantially concurrently etching said first material layer and said stress buffer material at substantially the same rate so as to expose said surface of said semiconductor device structure adjacent said at least one recess with said surface of said semiconductor device structure and a surface of said first material layer in said at least one recess being located in substantially the same plane following said planarizing.

82. A spin coating method, comprising:
applying a material to a substrate;
spinning said substrate and said material at a first speed;
decreasing a rate of said spinning to a second speed; and
gradually increasing a rate of said spinning to a third speed.

83. The method of claim 82, wherein said spinning said substrate and said material at said first speed comprises substantially filling recesses formed in said substrate with said material.

84. (Amended) The method of claim 82, wherein said decreasing said rate and spinning said substrate and said material at said second speed comprise permitting said material located within recesses formed in said substrate to set.

85. The method of claim 82, wherein spinning said substrate and said material at said third speed comprises forming said material over a surface of said substrate to a desired thickness.

86. (Amended) The method of claim 82, wherein said decreasing said rate follows said spinning.

87. The method of claim 84, wherein said gradually increasing said rate follows said decreasing said rate.

88. (Amended) A semiconductor device structure with a substantially planar surface, comprising:
a substrate including at least one recess formed therein; and
a material layer disposed over said substrate and substantially filling said at least one recess, said material layer having a substantially planar surface free of abrasive planarization-induced defects.

89. (Amended) The semiconductor device structure of claim 88, wherein said substrate comprises a semiconductor substrate with a surface and said at least one recess comprises at least one trench recessed in said surface of said semiconductor substrate.

90. The semiconductor device structure of claim 88, wherein said material layer comprises a mask material.

91. (Amended) The semiconductor device structure of claim 90, further comprising at least one conductively doped region continuous with a surface of said semiconductor substrate and laterally adjacent said at least one trench.

92. (Amended) The semiconductor device structure of claim 88, wherein said substrate comprises:

a shallow trench isolation structure including a semiconductor substrate with a surface and at least one trench formed in said surface of said semiconductor device substrate; and

an insulator layer substantially filling said at least one trench and covering said surface of said semiconductor device substrate.

93. (Amended) The semiconductor device structure of claim 92, wherein said insulator layer includes a nonplanar upper surface with at least one peak located substantially above said surface of said semiconductor device substrate and at least one valley located substantially above said at least one trench.

94. The semiconductor device structure of claim 93, wherein said material layer comprises a stress buffer layer that substantially fills said at least one valley in said insulator layer.

95. (Amended) The semiconductor device structure of claim 88, wherein said substrate comprises:

a semiconductor device structure including a surface with at least one dual damascene trench formed thereon; and

a conductive layer substantially filling said at least one dual damascene trench and covering said surface of said semiconductor device structure.

96. (Amended) The semiconductor device structure of claim 95, wherein said conductive layer includes a nonplanar upper surface with at least one peak located substantially above said surface of said semiconductor device structure and at least one valley located substantially above said at least one dual damascene trench.

97. (Amended) The semiconductor device structure of claim 96, wherein said material layer comprises a stress buffer layer that substantially fills said at least one valley in said conductive layer.

98. The semiconductor device structure of claim 88, wherein said substrate comprises a stacked capacitor structure including an insulator layer with at least one container recessed therein.

99. The semiconductor device structure of claim 98, wherein said material layer comprises a mask material, said mask material substantially filling said at least one container.

100. (Amended) The semiconductor device structure of claim 99, wherein mask material covering a surface of said insulator layer has a thickness of less than a height of said at least one container.

101. (Amended) The semiconductor device structure of claim 99, wherein mask material covering a surface of said insulator layer has a thickness of less than about half a depth of said at least one container.